What is claimed is:

1. A method of forming a contact opening through a dielectric layer overlaying an oxide layer in an integrated circuit, the method comprising:

forming a layer of mask material overlaying the dielectric layer;

patterning the layer of mask material to expose a pre-selected portion of the dielectric layer; and

forming anisotropic contact openings that extend through the layer of dielectric and the layer of oxide using a dry etch with a single mask.

2. The method of claim 1, further comprising:

removing the layer of mask material.

3. The method of claim 1, wherein the mask material is photo resist mask material.

4. The method of claim 1, wherein the pattering of the layer of mask material further comprises:

removing a portion of the mask material adjacent a portion of the dielectric layer where the contact opening is to be formed.

5. The method of claim 1, wherein the dry etch used is a reactive ion dry etch.

6. The method of claim 1, wherein the dry etch used is a plasma etch.

7. The method of claim 1, wherein the dry etch used is an ion beam milling etch.

8. The method of claim 1, wherein the dielectric constant of the dielectric layer is higher than the dielectric constant of the layer of oxide.

9. The method of claim 1, wherein the dielectric is silicon nitride (nitride).

10. A method of forming an integrated circuit, the method comprising:

forming an oxide layer on a surface of a substrate, the substrate having a plurality of isolation islands, wherein at least one isolation island is used in forming a semiconductor device;

patterning the oxide layer to expose predetermined areas of the surface of the substrate;

depositing a nitride layer overlaying the oxide layer and the exposed surface areas of the substrate; and

implanting ions through the nitride layer, wherein the nitride layer is an implant screen for the implanted ions.

11. The method of claim 10, further comprising:

diffusing the ions to form device regions in selected isolation islands in the substrate.

12. The method of claim 10, further comprising:

using the nitride layer in at least one of the isolation islands as a capacitor dielectric in forming a capacitor.

13. The method of claim 10, further comprising:

performing a dry etch to form anisotropic contact openings that extend through the layer of nitride and through the layer of oxide to access selected device regions formed in the substrate.

14. The method of claim 13, wherein the dry etch used is a reactive ion dry etch.

15. A method of forming an integrated circuit, the method comprising:

forming an oxide layer on a surface of a substrate, the substrate having a plurality of isolation islands, wherein at least one isolation island is used in forming a semiconductor device of the integrated circuit;

patterning the oxide layer to expose predetermined areas of the surface of the substrate;

depositing a dielectric layer overlaying the oxide layer and the exposed surface areas of the substrate, wherein the dielectric layer has a higher dielectric constant than a dielectric constant of the oxide layer;

implanting ions through the dielectric layer;

diffusing the ions to form device regions in selected isolation islands in the substrate; and

using the dielectric layer in at least one of the isolation islands as a capacitor dielectric in forming a capacitor.

16. The method of claim 15, wherein the capacitor dielectric layer is a layer of silicon nitride.

17. The method of claim 15, further comprising:

forming contact openings to the device regions.

18. The method of claim 17, wherein forming the contact openings further comprises:

using a dry etch to selectively form contact openings through the dielectric layer and the oxide layer to expose selective areas of device regions formed in the substrate under the dielectric layer and the oxide layer.

19. The method of claim 18, wherein the dry etch forms generally vertical sidewalls in the contact opening with respect to the surface of the substrate.

20. The method of claim 17, further comprising:

depositing a layer of metal overlaying the layer of nitride and the exposed device regions through the contact openings; and

patterning the layer of metal contacts to form metal contact regions for each contact opening.

21. The method of claim 15, wherein the implanting and the diffusing of the ions creates a bottom plate of the MOS capacitor in an associated isolation island.

22. The method of claim 21, wherein forming the MOS capacitor further comprises:

depositing a layer of metal overlaying the dielectric layer and an associated contact opening; and

patterning the metal layer to form a top plate and a bottom plate contact region, wherein the bottom plate contact region is in contact with the bottom plate through the contact opening.

23. A method of forming an integrated circuit, the method comprising:

forming a first oxide layer on a surface of a substrate, the substrate having a plurality of isolation islands, wherein at least one isolation island is used in forming a semiconductor device of the integrated circuit;

patterning the first oxide layer to expose predetermined areas of the surface of the substrate;

implanting and diffusing ions into the substrate to form device regions;

forming a dielectric layer overlaying the oxide layer and the exposed areas of the surface of the substrate, wherein the dielectric layer has a dielectric constant higher than a dielectric constant of the oxide layer; and

using the dielectric layer in at least one of the isolation islands as a capacitor dielectric in forming a capacitor.

24. The method of claim 23, wherein the dielectric layer is a nitride layer formed by low pressure chemical vapor deposition.

25. The method of claim 23, further comprising:

using open tube deposition as a dopant source to form the device regions.

26. The method of claim 25, wherein the dopant source is phosphorus oxychloride.

27. The method of claim 25, wherein a non-selective etch is used to expose the surface of the semiconductor adjacent device regions before the dielectric layer is formed.

28. The method of claim 25, wherein the etchant used is a wet etchant containing hydrogen fluoride.

29. The method of claim 23, further comprising:

forming contact openings to the device regions.

30. The method of claim 29, wherein forming the contact openings further comprises:

using a dry etch to selectively form contact openings through the dielectric layer and the oxide layer to expose selective areas of device regions formed in the substrate under the capacitor dielectric layer and the oxide layer.

31. The method of claim 29, wherein one of device regions formed in the isolation island containing the capacitor is a bottom plate and one of the contact openings is formed through the dielectric layer to expose a portion of the bottom plate.

32. The method of claim 31, wherein the forming of the capacitor further comprising:

depositing a layer of metal overlaying the dielectric layer and the contact opening to the bottom plate; and

patterning the metal layer to form a top plate and a bottom plate contact region, wherein a portion of the dielectric layer is positioned between bottom plate and the top plate and the bottom contact region is in contact with the bottom plate through the contact opening to the bottom plate.

33. A method of forming a capacitor and a transistor in an integrated circuit, the method comprising:

forming a plurality of isolation islands in a substrate of a first conductivity type with low dopant density, wherein the substrate contains a capacitor isolation island to form the capacitor in and a transistor isolation island to form the transistor in;

forming a base of a second conductivity type in the transistor isolation island adjacent a surface of the substrate;

forming a layer of oxide on a surface of the substrate;

patterning the layer of oxide to form pre-selected exposed surface areas of the substrate;

forming a layer of dielectric over the layer of oxide and the exposed surface areas of the substrate;

implanting dopants of the first conductivity type with high dopant density through the layer of dielectric into the substrate;

diffusing the dopants to form a bottom plate in the capacitor isolation island and an emitter and collector contact in the transistor isolation island, wherein the emitter is formed in a portion of the base, further wherein the bottom plate, the emitter and the collector contact are formed adjacent the surface of the substrate;

using a dry etch to form contact opening through the dielectric layer to the bottom plate in the capacitor isolation island;

using a dry etch to form a contact opening through the dielectric layer and the oxide layer to the emitter in the transistor isolation island;

using a dry etch to form a contact opening through the dielectric layer to the collector contact in the transistor isolation island;

forming a layer of metal overlaying the dielectric layer and the contact openings; and

etching the layer of metal to form a top plate and a bottom plate contact region in the capacitor isolation region and an emitter contact region and a collector contact region in the transistor isolation region.

34. The method of claim 33, wherein the dielectric layer is used an implant screen in implanting the dopants into the respective isolation islands.

35. The method of claim 33, wherein a portion of the patterned dielectric layer is used as the capacitor dielectric in forming the capacitor.

36. The method of claim 33, wherein the dielectric layer is a nitride layer.

37. The method of claim 36, wherein the nitride layer is formed by low pressure chemical vapor deposition.

38. An integrated circuit comprising:

a substrate having a plurality of isolation islands, wherein at least one isolation island has a semiconductor device formed therein;

a layer of oxide formed and patterned on a surface of the substrate;

a layer of dielectric formed overlaying the layer of oxide and exposed surface areas of the substrate, the layer of dielectric having a dielectric constant that is higher than the dielectric constant of the layer of oxide, wherein the dielectric layer is used as an implant screen in implanting dopants into respective isolation islands to form devices regions; and

at least one capacitor formed in one of the isolated island in the substrate, each capacitor using the layer of dielectric as a capacitor dielectric, each capacitor dielectric is positioned between a top plate and a bottom plate of an associated capacitor.

39. The integrated circuit of claim 38, further comprising:

the layer of dielectric and the layer of oxide having anisotropic device openings to expose device regions in the substrate, wherein the device openings are formed by a dry etch.

40. The integrated circuit of claim 39, wherein the dry etch used is a reactive ion etch.

41. The method of claim 38, wherein the layer of dielectric is a layer of nitride.

42. The method of claim 41, wherein the nitride layer is formed by low pressure chemical vapor deposition.

43. An integrated circuit comprising:

a substrate of having a plurality of isolation islands, wherein at least one isolation island has a semiconductor device formed therein;

a layer of oxide formed and patterned on a surface of the substrate;

a layer of dielectric formed overlaying the layer of oxide and exposed surface areas of the substrate, wherein the layer of dielectric has a dielectric constant that is higher than the dielectric constant of the layer of oxide;

the layer of dielectric and the layer of oxide having anisotropic device openings to expose device regions in the substrate, wherein the device openings are formed by a dry etch; and

at least one capacitor formed in one of the isolated islands in the substrate, each capacitor using the layer of dielectric as a capacitor dielectric, each capacitor dielectric is positioned between a top plate and a bottom plate of an associated capacitor.

44. The integrated circuit of claim 43, wherein the dielectric layer is used an implant screen in implanting dopants into the respective isolation islands to form the device regions.

45. The integrated circuit of claim 43, wherein the dry etch used is a reactive ion etch.

46. The method of claim 43, wherein the layer of dielectric is a layer of nitride.

47. The method of claim 46, wherein the nitride layer is formed by low pressure chemical vapor deposition.

48. An integrated circuit comprising:

a substrate having a surface and a plurality of isolation islands;

one or more semiconductor devices, each semiconductor device is formed in an associated isolation island, some of the semiconductor devices having device regions formed adjacent the surface of the substrate;

an oxide layer formed and patterned on the surface of the substrate;

a dielectric layer overlaying the patterned oxide layer and exposed surface areas of the substrate, wherein the layer of dielectric has a dielectric constant that is higher than the dielectric constant of the layer of oxide;

the oxide and dielectric layers over select device regions having contact openings with generally vertical side walls with respect to the surface of the substrate; and

at least one capacitor formed in one of the isolation islands, the capacitor having a capacitor dielectric that is formed from a portion of the dielectric layer.

49. The integrated circuit of claim 48, further comprising:

a metal contact region formed in each contact opening to provide a contact to the associated device region.

50. The integrated circuit of claim 48, wherein one of the at least one capacitor, further comprising:

a bottom plate formed in the substrate; and

a top plate overlaying the dielectric layer, wherein the dielectric layer positioned between the top plate and the bottom plate is the capacitor dielectric.

51. The integrated circuit of claim 48, wherein the layer of dielectric is a layer of nitride.

52. The integrated circuit of claim 48, wherein a portion of the dielectric layer has a contact opening to the bottom plate.

53. The integrated circuit of claim 48, further comprising:

a bottom plate contact region formed in the contact opening to the bottom plate.

54. The integrated circuit of claim 48, wherein one of the semiconductor devices in an isolation island is a transistor, further comprising:

a base region formed in the isolation island adjacent the surface of the substrate;

a emitter formed in the base region adjacent the surface of the substrate; and

a collector contact formed in the isolation island adjacent a surface of the substrate.

55. The integrated circuit of claim 54, wherein a portion of the dielectric and oxide layers covering the base region has a contact opening that extends to the base region.